

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated November 3, 2005 (U.S. Patent Office Paper No. 20051028). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1-15 stand for consideration in this application, wherein claims 1-4, 8 and 10-13 are being canceled without prejudice or disclaimer, while claims 5-7, 9, and 14 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. Support for the modifications of claim 5-6 may be found on p. 20, line 21 – p.22, line 1, Furthermore, support for the modification of claim 7 may be found on p.22, line 2- p.17 of the Specification. In addition, new claims 16 and 17 are hereby submitted for consideration. Support for the new claims 16 and 17 may be found on p. 10 lines 5- 12, and p. 11, lines 6-9 of the Specification, Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formal Rejections

Claims 3 and 4 were rejected under 35 U.S.C. §112, second paragraph, for being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 4 are now being canceled. Therefore, withdrawal of this rejection is respectfully requested.

Prior Art Rejections

The First 35 U.S.C. §102 (b) rejection

The Office Action rejected claims 1, 2, 5, and 6 under 35 U.S.C. §102(b) as being anticipated by Bell et al. (U.S. Pat. No. 6,021,451) (hereinafter Bell). Claims 1 and 2 are being cancelled, and therefore claims 5 and 6 now stand rejection. Applicants respectfully traverse this rejection for the reasons set forth below.

According to the M.P.E.P. §2131, a claim is anticipated under 35 U.S.C. §102 (a), (b), and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior reference.

Claim 5

The Office Action specifically contends that Bell shows a semiconductor integrated circuit comprising; a first bus; a second bus; a data transfer device to transfer data between the first and second buses; a central processing unit connected to the first bus; and program storage memory which stores a control program for the central processing unit and is connected to the first bus, wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second bus by means of the data transfer device. Applicants respectfully disagree.

Bell shows a bus bridge between an IP bus and a processor bus which connects to processors of multiple agents for maintaining transaction ordering. Contrary to the Office Action, Bell does not show the bridge comprises a central processing unit. In contrast, claim 5 as amended recites that a semiconductor integrated circuit for controlling data transfer comprises a central processing unit connected to the first bus.

Furthermore, Bell does not show a bus bridge comprises a bus control unit. In contrast, claim 5 as amended recites that the semiconductor integrated circuit comprises a bus control unit controlling bus arbitration for the first bus and the second bus.

Furthermore, Bell merely shows that a transactional arbitration unit in the bus bridge maintains transaction ordering by determining whether requests can be placed in the inbound request queue and whether requests originating on the processor bus can be responded immediately or whether the agent originating the request must wait for a reply. In other words, Bell shows that a transaction ordering is controlled by placing a request in the request queue. However, Bell does not show that the bus bridge controls bus access by requesting a bus access right to a bus for reading/writing to the bus control unit and accessing the bus.

In contrast, claim 5 as amended recites that the data transfer unit requests a bus access right of one of the buses for reading to the bus control unit, and accesses the one bus for reading data, and releases the bus access right of the one bus, and requests a bus access right

of the other bus for writing to the bus control unit after releasing the bus access right of the one bus, and accesses the other bus for writing the data in response to one data transfer start request. In other words, the semiconductor integrated circuit of the present invention controls buses without placing a request of a bus access right in a request queue. Bell does not show such an element. Furthermore, Bell neither expressly nor inherently describes the apparatus recited in claim 5. Accordingly, claim 5 is not anticipated by Bell.

Claim 6

The Office Action specifically contends that Bell shows a semiconductor integrated circuit comprising: a first bus; a second bus; a data transfer device to transfer data between the first and second buses; a central processing unit connected to the first bus; and a bus control means for the first and second buses, wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first and second buses independently. Applicants respectfully disagree.

As mentioned above, the bridge in Bell does not comprise a central processing unit connected to a bus and a bus control unit. In contrast, claim 6 as amended recites that a semiconductor integrated circuit for controlling data transfer comprises a central processing unit connected to the first bus and a bus control unit.

Furthermore, as mentioned above, Bell merely shows that a transaction ordering is controlled by placing a request in the request queue. In contrast, claim 6 as amended recites that the data transfer unit independently requests a bus access right and output an address to the first bus and the second bus according to a data transfer start request, requests a bus access right of one of the buses for reading to the bus control unit, accessing the one bus according to the bus access right of one bus, and release the bus access right of one bus, and requests a bus access right of the other bus for writing after accessing the one bus for reading. Bell does not show such an element. Furthermore, Bell neither expressly nor inherently describes the apparatus recited in claim 6. Accordingly, claim 6 is not anticipated by Bell.

Second 35 U.S.C. §102 (b) rejection

The Office Action rejected claims 7-15 under 35 U.S.C. §102(b) as being anticipated by Olarig, U.S. Pat. No. 6,567,880 B1. Claims 8 and 10-13 are being cancelled, and therefore only claims 7 and 14-15 stand rejection. Applicants respectfully traverse this rejection for the reasons set forth below.

Claim 7

The Office Action specifically contends that Olarig shows A semiconductor integrated circuit comprising: a first bus; a second bus; a third bus; a central processing unit connected to the first bus; program storage memory which stores a control program for the central processing unit and is connected to the first bus; and a data transfer device capable of data transfer between the second bus and the third bus, wherein the data transfer device can independently request a bus access right and output an address to the second bus and the third bus, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device the bus control unit is capable of arbitration of bus access right requests and bus control for the first bus, the second bus, and the third bus independently. The Office Action further contends that the PCI/PCI bridge operates such that PCI bus and AGP bus can exchange data, and the various arbiters and control elements for reading data from one bus and writing the data to another bus, and this is the function of any bus bridge. Applicants respectfully disagree.

Claim 7 as amended comprises an element of “a bus control unit for controlling the first bus, the second bus, and the third bus.” Olarig merely shows that PCI/PCI bridge controls two buses. Olarig does not show that PCI/PCI bridge controls three buses. Furthermore, claim 7 as amended comprises a data transfer device that requests a bus access right of one bus for reading and accesses to one bus according to the bus access right, and release the bus access right of one bus, and request a bus access right of the other bus for writing in response to one data transfer start request. Olarig does not show such an element. Furthermore, Olarig neither expressly nor inherently describes the apparatus recited in claim 7. Accordingly, claim 7 is not anticipated by Olarig.

Claims 14-15

Claims 14-15 are dependent upon the independent claim 7. As to dependent claims 14-15, the argument set forth above is equally applicable here. The base claim is allowable, dependent claims 14-15 must also be allowable.

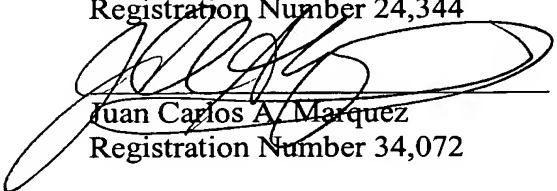
Conclusion

In view of all the above, Applicant respectfully submits that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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